

ST STM32G491 :: ARM Cortex M4

The [ST STM32G491](#) are high-performance Arm Cortex-M4 32-bit MCUs running up to 170 MHz, with FPU, DSP instructions, and MPU for security. They feature up to 512 KB Flash, 112 KB SRAM, Quad-SPI interface, and extensive I/Os on multiple buses. Memory protection includes read/write safeguards and secure areas. Hardware acceleration is provided via CORDIC and FMAC units. Peripherals include three 12-bit ADCs, four DACs, four comparators, voltage reference, RTC, multiple 16- and 32-bit timers, and PWM timers for motor control.

The BSP development is made with ST Nucleo-G491RE development board. The BSP features a CMake build system, GCC toolchain supports and built based on our Hardware Abstraction Layer (HAL). It requires an application configuration file, which allows the user to specify the CPU clock frequency, enable or disable RTOS, and further define project-level I/O and settings.

The software is architected with long-term maintainability and adherence to high software quality standards as core design principles.

- ✔ Layered architecture with clear HAL abstraction
- ✔ Conforms to ISO C99 standard
- ✔ Supports both RTOS and bare-metal environments
- ✔ CMake build system for scalable integration
- ✔ Seamless integration with GCC toolchain
- ✔ Statically analyzed for MISRA, CERT, and CWE compliance

Features	Remarks
FPU support	Yes
Max. clock speed	170 MHz
Flash size	512 kB
SRAM	112 kB

Peripherals	Total Channels
ADC	18
DAC	4
GPIO	52
FDCCAN	2
I2C	3
NVM	-
PWM	3
RTCC	1
SPI	3
Timer	7
UART	3

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BSP_STM32G491

PUBLIC

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Passed

Last analysis: 28 seconds ago • 4.7k Lines of Code • C

A 0

Security

A 0

Reliability

A 0

Maintainability

A —

Hotspots Reviewed

0.0%

Coverage

0.0%

Duplications

Support Package:

LQFP64, UFQFPN32