NXP LPC845 :: ARM Cortex M0+

The NXP LPC845 is a low-cost Arm Cortex-M0+ 32-bit MCU family running up to 30 MHz, with up to 64 KB Flash and 16 KB SRAM. It includes multiple communication interfaces (I2C, USART, SPI), capacitive touch support, various timers (MRT, SCTimer/PWM, 32-bit timer), DMA, 12-bit ADC, dual 10-bit DACs, analog comparator, CRC engine, flexible switch matrix for I/O configuration, pattern match engine, and up to 42 GPIO pins.

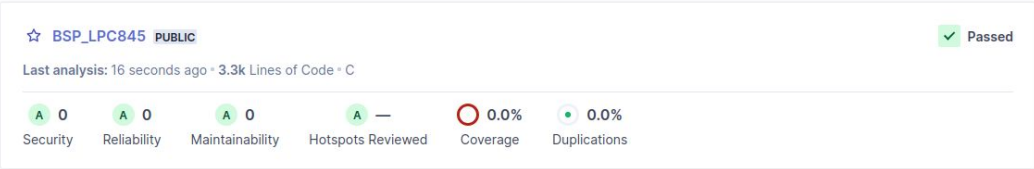
The BSP development is made with a NXP LPC845-BRK development board. The BSP features a CMake build system, GCC toolchain supports and built based on our Hardware Abstraction Layer (HAL). It requires an application configuration file, which allows the user to specify the CPU clock frequency, enable or disable RTOS, and further define project-level I/O and settings.

The software is architected with long-term maintainability and adherence to high software quality standards as core design principles.

✅ Layered architecture with clear HAL abstraction
✅ Conforms to ISO C99 standard
✅ Supports both RTOS and bare-metal environments
✅ CMake build system for scalable integration
✅ Seamless integration with GCC toolchain
✅ Statically analyzed for MISRA, CERT, and CWE compliance

Features	Remarks
FPU support	No
Max. clock speed	30 MHz
Flash size	64 kB
SRAM	16 kB

Peripherals	Total Channels
ADC	12
DAC	2
GPIO	42
I2C	4
PWM	7
SPI	2
Timer	4
UART	3



Support Package:
LQFP48