# ST STM32C011 :: ARM Cortex M0+

The ST STM32C011 is a low-cost Arm Cortex-M0+ 32-bit MCU running up to 48 MHz, with up to 32 KB Flash and 6 KB SRAM. It includes communication interfaces such as I2C, SPI/I2S, and USART, along with DMA, MPU, and multiple timers. Additional peripherals include a 12-bit ADC (up to 2.5 MSPS), RTC, watchdog timers, enhanced GPIO, low-power modes, and support for packages ranging from 8 to 20 pins.

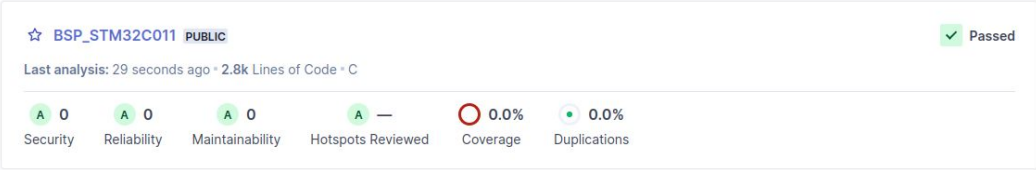
The BSP development is made with ST STM32C0116-DK development board. The BSP features a CMake build system, GCC toolchain supports and built based on our Hardware Abstraction Layer (HAL). It requires an application configuration file, which allows the user to specify the CPU clock frequency, enable or disable RTOS, and further define project-level I/O and settings.

The software is architected with long-term maintainability and adherence to high software quality standards as core design principles.

✅ Layered architecture with clear HAL abstraction
✅ Conforms to ISO C99 standard
✅ Supports bare-metal environments
✅ CMake build system for scalable integration
✅ Seamless integration with GCC toolchain
✅ Statically analyzed for MISRA, CERT, and CWE compliance

| Features | Remarks |
|---|---|
| FPU support | No |
| Max. clock speed | 48 MHz |
| Flash size | 32 kB |
| SRAM | 6 kB |

| Peripherals | Total Channels |
|---|---|
| ADC | 13 |
| GPIO | 18 |
| I2C | 1 |
| PWM | 6 |
| RTCC | 1 |
| SPI | 1 |
| Timer | 5 |
| UART | 2 |




Support Package:
**UFQFPN20**